Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A semiconductor integrated circuit comprising a plurality of combinational logic components, a memory and a testing arrangement for configuring the memory prior to testing the combinational logic components using one or more scan chains, the arrangement comprising:

a data generator for generating a predetermined bit pattern for writing to the memory;

a switching arrangement for selectively switching the memory input to receive data from the combinational logic components or from the data generator; wherein

the switching arrangement and data generator are arranged to input the predetermined bit pattern to the memory prior to testing the integrated circuit.

2. (Original) A semiconductor integrated circuit according to claim 1, the arrangement further comprising an enable input, the enable input being arranged to prevent writing to the memory after writing the predetermined bit pattern to memory.

3. (Original) A semiconductor integrated circuit according to claim 1, wherein the bit pattern for a given address comprises a function of the address bit sequence, and wherein the data generator is arranged to present the bit pattern at outputs corresponding to address inputs of the memory.

4. (Original) A semiconductor integrated circuit according to claim 1, the arrangement further comprising an arrangement of multiplexers to selectively connect the memory to the combinational logic components of the integrated circuit, or to the data generator.

5. (Original) A semiconductor integrated circuit according to claim 1, the arrangement further comprising an address generator for generating addresses of the memory to which the bit pattern is to be written, the data generator comprising an array of interconnections for transferring the address bit sequence from the address generator to a data input of the memory.

6. (Original) A semiconductor integrated circuit according to claim 1, wherein the pattern is a checkerboard pattern in the memory.

7. (Original) A semiconductor integrated circuit according to claim 1, wherein the pattern is so arranged that the RAM may be modeled as a simple combinational circuit.

8. (Original) A semiconductor integrated circuit according to claim 1, wherein the arrangement comprises a wrapper circuit for selectively preloading the memory, or for connecting the memory to other components in the integrated circuit.

9. (Original) A semiconductor integrated circuit according to claim 1, wherein the arrangement comprises a wrapper circuit and includes a control for selectively controlling the memory to behave as a ROM after writing the bit pattern to memory, and while testing the integrated circuit.

10. (Currently Amended) A semiconductor circuit comprising:

a memory array;

a plurality of logic elements selectively coupled to the memory array;

a data generator selectively coupled to the memory array for generating a predetermined bit pattern for writing to the memory;

a switching circuit for selectively coupling the logic elements or the data generator to input data into the memory array at a selected time under control of a control circuit.

11. (Original) The semiconductor circuit according to claim 10 wherein said switching circuit includes a multiplexer having one input coupled to the logic elements and another input coupled to the data generator and a control input coupled to the control circuitry to selectively connect the memory to the logic elements or to the data generator.

12. (Original) The semiconductor circuit according to claim 10 wherein said data generator creates a selected bit pattern for loading into the memory array prior to testing of the semiconductor circuit.

13. (Original) The semiconductor circuit according to claim 12 wherein the bit pattern which is selected for a given address in the memory array is a function of the address bit sequence.

14. (Original) The semiconductor circuit according to claim 10 in which the time selected for coupling the data generator to the memory array is prior to testing of the semiconductor circuit so that a predetermined bit pattern is input by the data generator into the semiconductor circuit prior to testing.

15. (Original) The semiconductor circuit according to claim 13 further comprising:

an address generator for generating addresses of the memory to which the bit pattern is to be written and the data generator includes an array of inner connections for transferring the address bit sequence from the address generator to a data input of the memory.

16. (Original) The semiconductor circuit according to claim 13 in which the bit pattern which is written to the memory is selected based on the type of memory to which the bit pattern is to be written.

17. (Original) The integrated circuit according to claim 16 wherein the memory is a RAM.

18. (Original) The semiconductor circuit according to claim 16 wherein the memory is a CAM.

19. (Original) The semiconductor circuit according to claim 10 wherein the control circuit selects a time for controlling input provided to the memory array and further including a memory array enable circuit to enable the input of data to the memory array prior to testing and to disable data input into the memory after a bit pattern has been written to the memory and during testing of the semiconductor circuit such that during testing, the memory array behaves as a ROM.

20. (New) A method of testing a semiconductor integrated memory circuit comprising:

switching a memory input with a multiplexer to receive address, data, and control signals, in a first state, from an external interface or, in a second state, from an internal address counter, an internal data generator and an internal test control circuit;

during the second state:

generating an address with the internal address counter for determining the address at which data will be written;

coupling an output of the internal address counter with an input of the internal data generator;

generating a predetermined bit pattern with the internal data generator based upon the value of the internal address counter;

writing the predetermined bit pattern into memory at the location specified by the internal address counter.

21. (New) A method of testing a semiconductor integrated memory circuit according to claim 20, wherein the predetermined bit pattern to be generated consists of a checkerboard pattern.

22. (New) A method of testing a semiconductor integrated memory circuit according to claim 21, wherein memory to be tested consists of a Content Addressable Memory.